1/6

FIG.1

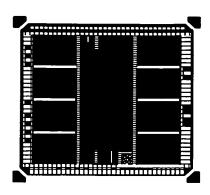
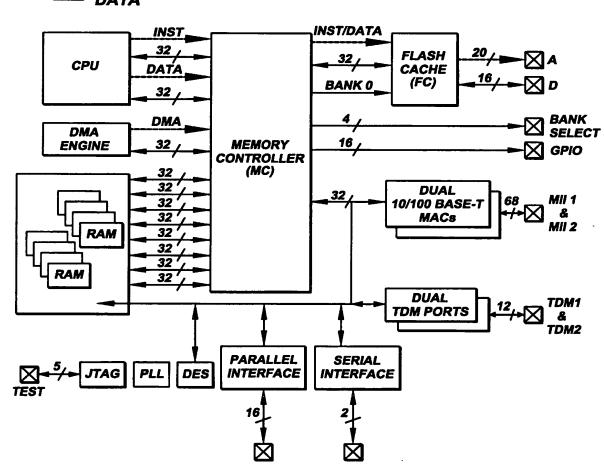


FIG.2

---- ADDRESS --- DATA

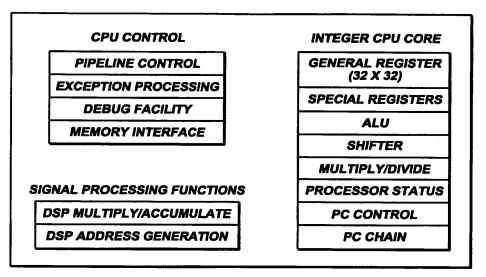


BEST AVAILABLE COPY

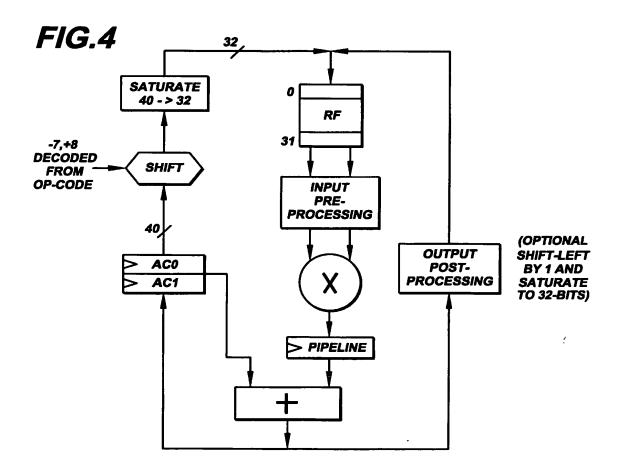


FIG.3

2/6



PIPELINE: IF RF EXE MEM WB
IF: INSTRUCTION FETCH, RF: REGISTER FETCH, EXE: EXECUTE, MEM: MEMORY ACCESS, WB: WRITE BACK





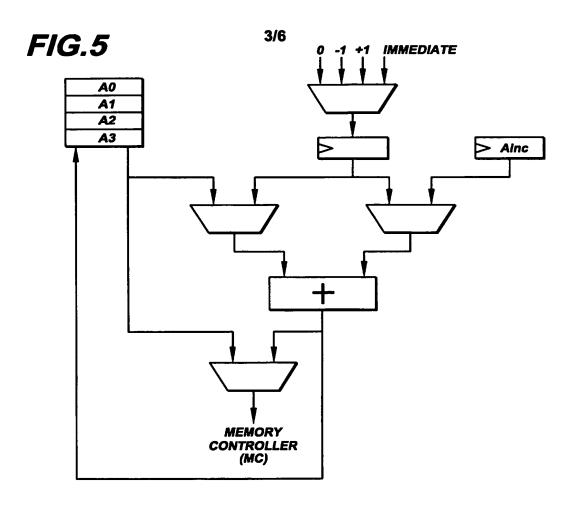
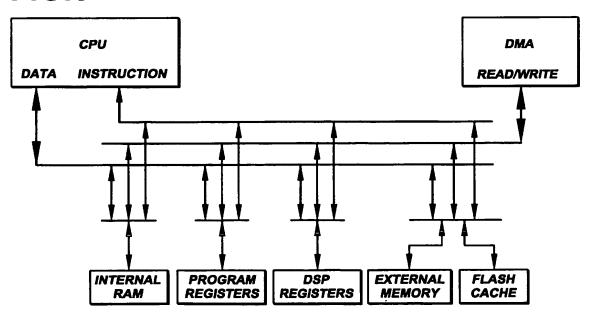


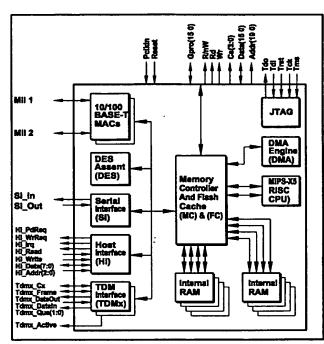
FIG.6





4/6

FIG.7



- MIPS-X5 Combined RISC and DSP core (200+ DSP MIPS).
- 256KBytes on chip RAM, 8 way interleaved, with single cycle access.
 64 Bytes of boot ROM.
- Two 10/100 Base T Ethernet MACs with MII interface.
- 8 KByte, 2 way set associative cache for external flash program memory.
- Glueless support of SLIC/SLAC codecs and character LCD displays via TDM & GPIO ports.
- GCC based compiler support with assembler and debugger.
- Low power. 1.8V +/- 10% core voltage, 3.3V +/- 10% I/O voltage.
- 176 TQFP package/JTAG.

FIG.8

- Software Development Tools
 - Dynamic linker, boot mechanism, compiler test suite, gdb/debug
- POSIX Operating System
 - Interrupt vector, context switching method, scheduling, semaphores, CLIB/printf
- Device Drivers
 - MAC, TDM, Host, UART
- Audio Libraries
 - G.711, G.723, G.729A, G.729E, Acoustic Echo Cancellation
- Managers
 - Audio, MAC/Network
- Applications
 - Audio loopback
 - MGCP/H3.23 loopback

5/6

FIG.9

- Implementation of the POSIX operating system
- Full support for:
 - Threads (single process, multiple threads)
 - Scheduling (two algorithms FIFO and round robin)
 - Semaphores
 - Mutexes
 - Condition Variables
 - Message Queues
 - Signal and Timers

FIG.10

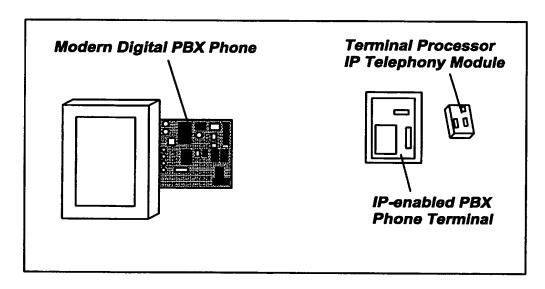




FIG.11

6/6

